CT25207

OPEN Alliance TC14 10BASE-T1S PMD Controller

Status

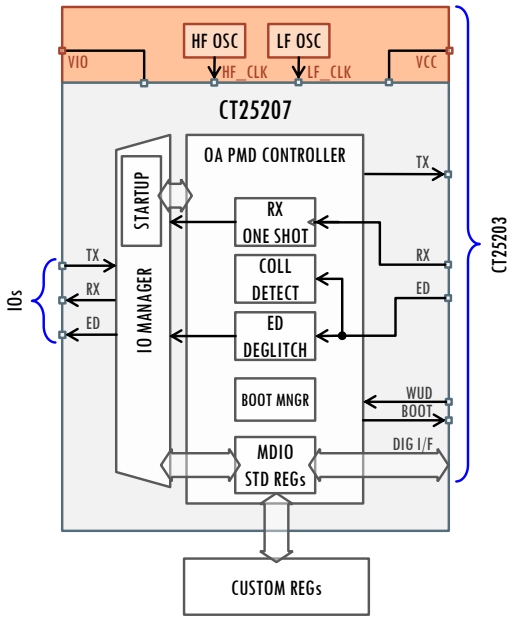
- Under development (silicon-proven by Q2-2023)

Deliverables

- RTL Object-Code
- Integration-level Verification Env. (UVM)
- Coverage Report
- SDC Constraints
- Integration Guide
- Test Specifications

Applications

- Automotive Networks
- Industrial Networks



Features

- Compliant to:
  - OPEN Alliance TC14 10BASE-T1S PMD I/F
  - OPEN Alliance TC14 Interoperability Specifications
  - OPEN Alliance TC14 System Implementation
  - OPEN Alliance TC10 Wake Up detection
  - OPEN Alliance TC14 Topology discovery
- Low Power consumption meeting OPEN Alliance TC10 requirement in sleep mode
- VCC supply 3.3V supply (±10%)
- VIO supply 2.5V or 3.3V (±10%)
- Voltage and current references, test infrastructures, included
- 10MHz (±30%) and 210MHz (±8%) input clocks for operation (oscillators available upon request in the target silicon process)

Description

The CT25207, in combination with the CT25203, implements a complete OPEN Alliance TC14 10BASE-T1S PMD Interface. The IP's tasks are:

- perform the boot sequence and drive the platform outside the IP to do the proper startup sequence after POR and after WAKE request
- recognize the encoded TX commands and keep updated the state of the PMD FSM after boot
- drive the platform outside the IP to do the shutdown sequence to enter LOWPOWER mode
- Filter ED and RX to fulfill the requirements of OPEN Alliance TC14 10BASE-T1S PMD I/F
- detect collisions on the line when transmitting and signal them on ED pin
- generate TX pulses for Topology Discovery with proper PRBS sequence
- perform WUT validation for wake-up

The IP also includes a MDIO slave that allows access to Clause 22 PMD standard registers and to IP specific registers (both embedded in the IP) and to custom registers (to be placed outside the IP).

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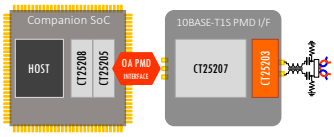
10BASE-T1S IPs

Frequently-Asked Questions

Q: Which kind of IC products I can develop using Canova Tech 10BASE-T1S silicon IPs solution?
A: Among others, here're some product examples you can develop with our 10BASE-T1S silicon IPs:

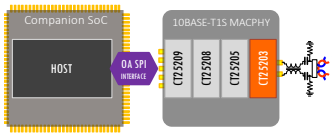
OPEN Alliance 10BASE-T1S PMD Interface IC + Companion SoC/FPGA



This 2-chip 10BASE-T1S networking solution mimics the CAN partition.

The **CT25203** Analog Front-End plus the **CT25207** PMD Controller are integrated, using BCD silicon technology process, in a single low pin-count tiny and low-cost chip.
By means of the standardized OPEN Alliance three-pin PMD Interface, it then connects to the SoC which integrates the Host, the **CT25208** Ethernet MAC, if needed, and the **CT25205** digital PHY in a pure digital silicon technology.

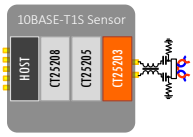
OPEN Alliance 10BASE-T1S MACPHY + Companion low-end MCU/FPGA



This innovative 2-chip 10BASE-T1S networking solution is based on the standardized OPEN Alliance SPI MACPHY Interface.

A single low pin-count, tiny "MACPHY" chip, made using BCD silicon technology process, integrates the **CT25203** Analog Front-End, the **CT25205** digital PHY, the **CT25208** Ethernet MAC and the **CT25209** SPI Protocol Handler. A low-end companion SoC/FPGA, is then connected to the MACPHY via a standard SPI interface.

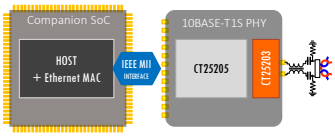
Sensor with integrated 10BASE-T1S interface



Automotive and Industrial sensors often integrate LIN and/or CAN interface in a single chip solution using BCD silicon technology.

The substitution of LIN and/or CAN interfaces with 10BASE-T1S Ethernet can be then realized by means of the **CT25203** Analog Front-End, the **CT25205** digital PHY and the **CT25208** Ethernet MAC directly connected to the Host Sensor in a similar way of LIN and/or CAN.

10BASE-T1S IEEE PHY + Companion Ethernet SoC



This is the "classical" Ethernet networking solution.

A standard 10BASE-T1S PHY integrates the **CT25203** Analog Front-End plus the **CT25205** digital PHY in a BCD silicon technology connecting, via the IEEE standard MII/MDIO Interface, to a companion Ethernet controller SoC. The world-first 10BASE-T1S PHY, in form of Test Chip vehicle and based upon the **CT25203** and the **CT25205**, has been released by Canova Tech in 2018. Have a look here for details.

Q: Are there any way to test the Canova Tech 10BASE-T1S silicon IPs solution?
A: Yes, by subscribing the "Early Access" program you can receive our development boards described here and the related technical support. Contact us for commercial details.

Q: Why the 10BASE-T1S front-end requires to be implemented on BCD technologies?
A: Because of the nature of the multi-drop network which obliges the silicon interface to expose high value of impedance to the line.
In fact, in presence of severe electromagnetic radiations induced on the twisted-pair, the line common-mode voltage can then reach the silicon with high-voltage peaks of ± tens of Volts. The BCD process ensure proper protection of the silicon against damages and avoid degradations of the quality of the communication in those severe conditions.
Contact us for checking if your target silicon process can be used for implementing the 10BASE-T1S front-end.

Q: May I ask Canova Tech to develop custom and dedicated analog and/or digital on top of the IPs?
A: Yes, you can. Our business model includes custom and dedicated Design Services to facilitate the integration of our IPs into your chip architecture. This business model includes the possibility for you to assign Canova the responsibility for design of a complete integrated circuit (GDS IP) based upon our IPs and your requirements.

Q: Is 10BASE-T1S protected by Standard-Essential Patents (like for CAN, 100BASE-T1, etc.)?
A: Yes, it is. the Physical-Layer Collision Avoidance Reconciliation sub-layer (clause 148 of the IEEE 802.3cg® standard) has been invented and patented by Canova Tech. We're always available to license it to you on the basis of FRAND (Fair, Reasonable and Non-Discriminatory) conditions already applied to several active licensee of Canova Tech's Intellectual Property Rights.
Contact us for setting the required NDA and receive the PLCA Patent Agreement.

Q: Which options do I have for licensing the Canova Tech 10BASE-T1S silicon IPs solution?
A: You can have several licensing options which includes:

- single-use/multiple-use license: the IPs (single or in bundle) are delivered as object-code and licensed for the use on a well-defined product code (single-use) or for unlimited product codes (multiple-use).
- architectural license: the IPs (single or in bundle) are delivered as source-code (plus know-how transfer) and licensed for the use on unlimited product codes.
- manufacturing license: here Canova Tech can develop your entire product, based upon our IPs (single or in bundle) and your product specifications. The GDS IP is licensed and delivered to you (including all necessary documentation and support) for you to manufacture your product and brand it.

Q: What kind of Support and IP Maintenance will I get from Canova?
A: You will get all required Support and IP Maintenance to ensure proper IP integration into your products for 12 months following the IP licensing. You can then subscribe, at your option, annual renewals of the Support and Maintenance agreement.

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