CT25205_TC

10BASE-T1S PHY/PMD Test Chip Vehicle

Description

The CT25205_TC is an IEEE 10BASE-T1S Physical Layer Transceiver supporting operation over a multi-drop network with at least 8 nodes and up to 25m of overall single twisted-pair cable length.
It supports MII to interface with a standard CSMA/CD compliant Ethernet MAC running at 10 Mb/s and the OPEN Alliance three-pin PMD Interface. It integrates the PLCA (**Physical Layer Collision Avoidance**) reconciliation sublayer functions to avoid physical collisions on the bus.
PLCA improves CSMA/CD performance in several ways:

- Guarantees that a packet transmitted by the MAC meets the line within a known time (bounded latency)
- Assigns transmit opportunities in a round-robin fashion to ensure fair access to the medium
- Maximizes throughput by avoiding collisions and MAC multiple back-off / retry
- Provides protection against the “babbling idiot” problem
- Allows for more robust operations in automotive EMC environment
- Integrating the PLCA RS in a single PHY chip allows existing SoC and MAC ICs to take advantage of PLCA

CT25205_TC Features

- Compliant to IEEE 802.3cg
- Integrated PLCA Reconciliation Sub-Layer
- Supports Short Reach Half-Duplex, Point-to-Point mode and Half-Duplex, Multi-Drop mode
- MII Interface support
- OA PMD Interface support
- MIIM (MDC/MDIO) Mngt Bus up to 2.5MHz
- Clause 45 Address Space
- Supports Clause 22 to Clause 45 access mode
- Interrupt Pin Option
- Robust Operation Over Single Twisted-Pair Automotive Cables
- Sustains OA DPI test @39dBm, maintaining a BER less than 10^{-10}
- Meets OA Automotive Emission Limits
- Single 5V power supply
- Adjustable 2.5V-5V I/O Supply
- Low Power < 200mW
- -40°C to 125°C Temp. range
- Experimental test chip not to be used in series production

36-pin QFN Package (6x6mm)

CT25205_TC Pinout

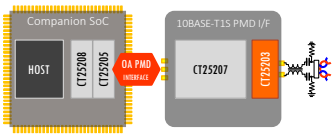
1	AIO0 Reserved test Pin	10	DIO1 General Purposes IO	19	TXD[0] MII Interface	28	RXER MII Interface
2	XTALO XTAL term	11	DIO0 General Purposes IO	20	TXD[1] MII Interface	29	RXDV MII Interface
3	XTALI XTAL term / ck input	12	MDINT MIIM interrupt signal	21	TXD[2] MII Interface	30	RXD[0] MII Interface
4	AVDDIN 5V Supply	13	RST Active Low Reset	22	TXD[3] MII Interface	31	RXD[1] MII Interface
5	PVDDIN 5V Supply	14	MDCK MDIO clock input	23	VDDIO 2.5V to 5.0V IO Supply	32	RXD[2] MII Interface
6	DRVVDD_P Internal LDO Output	15	MDIO MDIO open-drain IO	24	DVDD Internal LDO Output	33	RXD[3] MII Interface
7	LINEP Positive Line Pin	16	TXCK MII Clock	25	RXCK MII Interface	34	FSOURCE Reserved test Pin
8	LINEN Negative Line Pin	17	TXEN MII Interface	26	CRS MII Interface	35	AVDDIN 5V Supply
9	DRVDD_N Internal LDO Output	18	TXER MII Interface	27	COL MII Interface	36	AIO1 Reserved test Pin

10BASE-T1S IPs

Frequently-Asked Questions

Q: Which kind of IC products I can develop using Canova Tech 10BASE-T1S silicon IPs solution?
A: Among others, here're some product examples you can develop with our 10BASE-T1S silicon IPs:

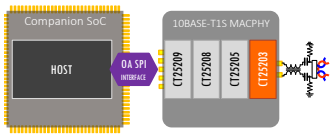
OPEN Alliance 10BASE-T1S PMD Interface IC + Companion SoC/FPGA



This 2-chip 10BASE-T1S networking solution mimics the CAN partition.

The **CT25203** Analog Front-End plus the **CT25207** PMD Controller are integrated, using BCD silicon technology process, in a single low pin-count tiny and low-cost chip.
By means of the standardized OPEN Alliance three-pin PMD Interface, it then connects to the SoC which integrates the Host, the **CT25208** Ethernet MAC, if needed, and the **CT25205** digital PHY in a pure digital silicon technology.

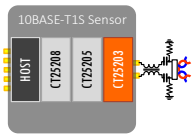
OPEN Alliance 10BASE-T1S MACPHY + Companion low-end MCU/FPGA



This innovative 2-chip 10BASE-T1S networking solution is based on the standardized OPEN Alliance SPI MACPHY Interface.

A single low pin-count, tiny "MACPHY" chip, made using BCD silicon technology process, integrates the **CT25203** Analog Front-End, the **CT25205** digital PHY, the **CT25208** Ethernet MAC and the **CT25209** SPI Protocol Handler. A low-end companion SoC/FPGA, is then connected to the MACPHY via a standard SPI interface.

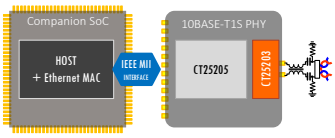
Sensor with integrated 10BASE-T1S interface



Automotive and Industrial sensors often integrate LIN and/or CAN interface in a single chip solution made using BCD silicon technology.

The substitution of LIN and/or CAN interfaces with 10BASE-T1S Ethernet can be then realized by means of the **CT25203** Analog Front-End, the **CT25205** digital PHY and the **CT25208** Ethernet MAC directly connected to the Host Sensor in a similar way of LIN and/or CAN.

10BASE-T1S IEEE PHY + Companion Ethernet SoC



This is the "classical" Ethernet networking solution.

A standard 10BASE-T1S PHY integrates the **CT25203** Analog Front-End plus the **CT25205** digital PHY in a BCD silicon technology connecting, via the IEEE standard MII/MDIO Interface, to a companion Ethernet controller SoC. The world-first 10BASE-T1S PHY, in form of Test Chip vehicle and based upon the **CT25203** and the **CT25205**, has been released by Canova Tech in 2018. Have a look here for details.

Q: Are there any way to test the Canova Tech 10BASE-T1S silicon IPs solution?
A: Yes, by subscribing the "Early Access" program you can receive our development boards described here and the related technical support. Contact us for commercial details.

Q: Why the 10BASE-T1S front-end requires to be implemented on BCD technologies?
A: Because of the nature of the multi-drop network which obliges the silicon interface to expose high value of impedance to the line. In fact, in presence of severe electromagnetic radiations induced on the twisted-pair, the line common-mode voltage can then reach the silicon with high-voltage peaks of ± tens of Volts. The BCD process ensure proper protection of the silicon against damages and avoid degradations of the quality of the communication in those severe conditions.
Contact us for checking if your target silicon process can be used for implementing the 10BASE-T1S front-end.

Q: May I ask Canova Tech to develop custom and dedicated analog and/or digital on top of the IPs?
A: Yes, you can. Our business model includes custom and dedicated Design Services to facilitate the integration of our IPs into your chip architecture. This business model includes the possibility for you to assign Canova the responsibility for design of a complete integrated circuit (GDS IP) based upon our IPs and your requirements.

Q: Is 10BASE-T1S protected by Standard-Essential Patents (like for CAN, 100BASE-T1, etc.)?
A: Yes, it is. the Physical-Layer Collision Avoidance Reconciliation sub-layer (clause 148 of the IEEE 802.3cg® standard) has been invented and patented by Canova Tech. We're always available to license it to you on the basis of FRAND (Fair, Reasonable and Non-Discriminatory) conditions already applied to several active licensee of Canova Tech's Intellectual Property Rights.
Contact us for setting the required NDA and receive the PLCA Patent Agreement.

Q: Which options do I have for licensing the Canova Tech 10BASE-T1S silicon IPs solution?
A: You can have several licensing options which includes:
- single-use/multiple-use license: the IPs (single or in bundle) are delivered as object-code and licensed for the use on a well-defined product code (single-use) or for unlimited product codes (multiple-use).
- architectural license: the IPs (single or in bundle) are delivered as source-code (plus know-how transfer) and licensed for the use on unlimited product codes.
- manufacturing license: here Canova Tech can develop your entire product, based upon our IPs (single or in bundle) and your product specifications. The GDS IP is licensed and delivered to you (including all necessary documentation and support) for you to manufacture your product and brand it.

Q: What kind of Support and IP Maintenance will I get from Canova?
A: You will get all required Support and IP Maintenance to ensure proper IP integration into your products for 12 months following the IP licensing. You can then subscribe, at your option, annual renewals of the Support and Maintenance agreement.