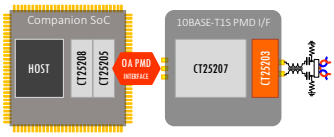
10BASE-T1S IPs

Frequently-Asked Questions

Q: which kind of IC products I can develop using the Canova's 10BASE-T1S silicon IPs solution?
A: among others, here're some product examples you can develop with our 10BASE-T1S silicon IPs:

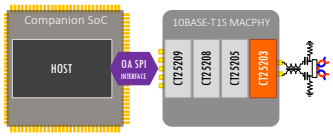
OPEN Alliance 10BASE-T1S PMD Interface IC + Companion SoC/FPGA



This 2-chip 10BASE-T1S networking solution mimic the CAN partition.

The **CT25203** Analog Front-End plus the **CT25207** PMD Controller are integrated, using BCD silicon technology process, in a single low pin-count tiny and low-cost chip.
By means of the standardized OPEN Alliance three-pin PMD Interface, it then connects to the SoC which integrates the Host, the **CT25208** Ethernet MAC, if needed, and the **CT25205** digital PHY in a pure digital silicon technology.

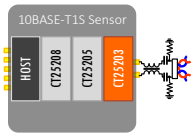
OPEN Alliance 10BASE-T1S MACPHY + Companion low-end MCU/FPGA



This innovative 2-chip 10BASE-T1S networking solution is based on the standardized OPEN Alliance SPI MACPHY Interface.

A single low pin-count, tiny "MACPHY" chip, made using BCD silicon technology process, integrates the **CT25203** Analog Front-End, the **CT25205** digital PHY, the **CT25208** Ethernet MAC and the **CT25209** SPI Protocol Handler. A low-end companion SoC/FPGA, is then connected to the MACPHY via a standard SPI interface.

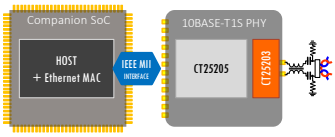
Sensor with integrated 10BASE-T1S interface



Automotive and Industrial sensors often integrate LIN and/or CAN interface in a single chip solution made using BCD silicon technology.

The substitution of LIN and/or CAN interfaces with 10BASE-T1S Ethernet can be then realized by means of the **CT25203** Analog Front-End, the **CT25205** digital PHY and the **CT25208** Ethernet MAC directly connected to the Host Sensor in a similar way of LIN and/or CAN.

10BASE-T1S IEEE PHY + Companion Ethernet SoC



This is the "classical" Ethernet networking solution.

A standard 10BASE-T1S PHY integrates the **CT25203** Analog Front-End plus the **CT25205** digital PHY in a BCD silicon technology connecting, via the IEEE standard MII/MDIO Interface, to a companion Ethernet controller SoC. The world-first 10BASE-T1S PHY, in form of Test Chip vehicle and based upon the **CT25203** and the **CT25205**, has been released by Canova Tech in 2018. Have a look here for details.

Q: are there any way to test the Canova's 10BASE-T1S silicon IPs solution?
A: yes, by subscribing the "Early Access" program you can receive our development boards described here and the related technical support. Contact us for commercial details.

Q: why the 10BASE-T1S front-end require to be implemented on BCD technologies?
A: because of the nature of the multi-drop network which oblige the silicon interface to expose high value of impedance to the line.
In fact, in presence of severe electromagnetic radiations induced on the twisted-pair, the line common-mode voltage can then reach the silicon with high-voltage peaks of ± tens of Volts. The BCD process ensure proper protection of the silicon against damages and avoid degradations of the quality of the communication in those severe conditions.
Contact us for checking if your target silicon process can be used for implementing the 10BASE-T1S front-end.

Q: may I ask Canova to develop custom and dedicated analog and/or digital on top of the IPs?
A: yes, our business model includes custom and dedicated Design Services to facilitate the integration of our IPs into your chip architecture. This business model includes the possibility for you to assign Canova the responsibility for design of a complete integrated circuit (GDS IP) based upon our IPs and your requirements.

Q: Is 10BASE-T1S protected by Standard-Essential Patents (like for CAN, 100BASE-T1, etc.)?
A: yes, the Physical-Layer Collision Avoidance Reconciliation sub-layer (clause 148 of the IEEE 802.3cg® standard) has been invented and patented by Canova Tech. We're always available to license it to you on the basis of FRAND (Fair, Reasonable and Non-Discriminatory) conditions already applied to several active licensee of Canova Tech's Intellectual Property Rights.
Contact us for setting the required NDA and receive the PLCA Patent Agreement.

Q: which options I do have for licensing the Canova's 10BASE-T1S silicon IPs solution?
A: You can have several licensing options which includes:

- single-use/multiple-use license: the IPs (single or in bundle) are delivered as object-code and licensed for the use on a well-defined product code (single-use) or for unlimited product codes (multiple-use).
- architectural license: the IPs (single or in bundle) are delivered as source-code (plus know-how transfer) and licensed for the use on unlimited product codes.
- manufacturing license: here Canova develop your entire product, based upon our IPs (single or in bundle) and your product specifications. The GDS IP is licensed and delivered to you (including all necessary documentation and support) for you to manufacture your product and brand it.

Q: what kind of Support and IP Maintenance will I get from Canova?
A: you will get all required Support and IP Maintenance to ensure proper IP integration into your products for 12 months following the IP licensing. You can then subscribe, at your option, annual renewals of the Support and Maintenance agreement.

CT25203

IEEE 802.3cg® 10BASE-T1S Analog Front-End

Status

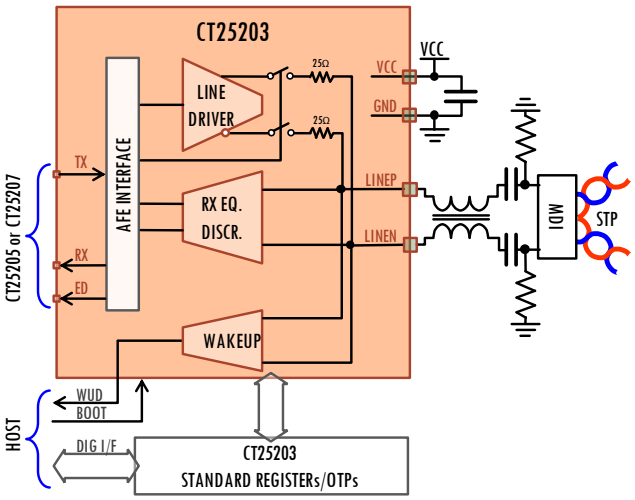
- Silicon-Proven (BCD silicon processes)
- Fully characterized
- EMI tested
- In mass production

Deliverables

- Datasheet
- GDS2 and LVS Netlist
- Footprint (.LEF)
- Test Specifications
- Integration guidelines
- Reference Design

Applications

- Automotive Networks
- Industrial Networks



Features

- Compliant to:
  - IEEE 802.3cg® specifications
  - OPEN Alliance TC14 Interoperability Specifications
  - OPEN Alliance TC14 EMC Specifications
  - OPEN Alliance TC14 System Implementation
- One-fits-all Analog Macro for implementing:
  - IEEE 802.3cg® 10BASE-T1S Physical Layer
  - OPEN Alliance TC6 10BASE-T1S MACPHY
  - OPEN Alliance TC14 10BASE-T1S PMD I/F
- Single min 3.3V supply
- Low Power consumption meeting OPEN Alliance TC10 requirement in sleep mode
- OPEN Alliance TC10 Wake Up detection
- Voltage and current references, test infrastructures, included
- Supply regulators, 25MHz XTAL and x4 (100MHz) DLL available upon request in the target silicon process.

Description

The CT25203 implements the analog front end of an IEEE 802.3cg® 10BASE-T1S physical layer.

It can be used in conjunction to other analog and digital blocks like (a) the CT25205 to implement a complete physical layer ethernet device, (b) the CT25207 to implement a complete OPEN Alliance PMD Interface and (c) the CT25209, the CT25208 and the CT25205 to implement a complete OPEN Alliance MACPHY (see next page for details).

The CT25203 has been designed in GlobalFoundries 130n-BCD process but also successfully and timely ported in other BCD silicon process technologies.

Availability of a complete IEEE physical layer Test Chip vehicle (CT25205_TC) and Evaluation Boards.

The BCD process is required to meet all EMI directives to be used in the Automotive and Industrial environments.

CT25205

IEEE 802.3cg® 10BASE-T1S Digital Controller

Status

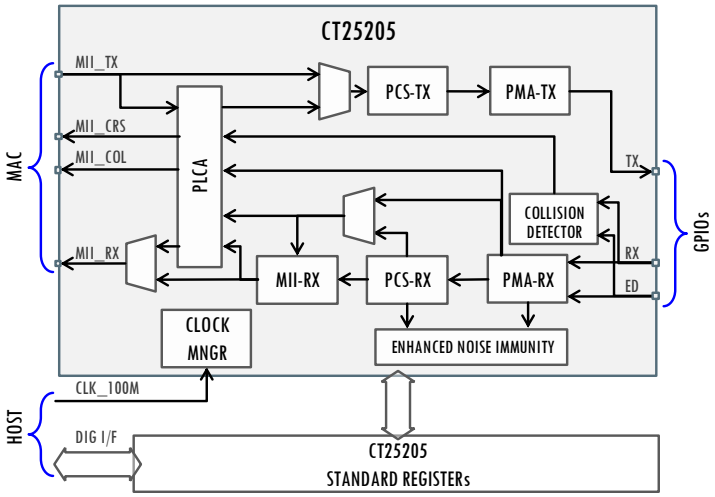
- Silicon-Proven
- Fully characterized
- EMI tested (in combination w/ CT25203)
- In mass production

Deliverables

- RTL Object-Code
- Integration-level Verification Env. (UVM)
- Protocol Compliance & Coverage Report
- SDC Constraints
- Integration Guide

Applications

- Automotive Networks
- Industrial Networks



Features

- Compliant to:
  - IEEE 802.3cg® specifications
  - OPEN Alliance TC14 PMD Transceiver INTERFACE
  - OPEN Alliance TC10 Sleep Wake Up
  - OPEN Alliance TC14 PLCA Diag.
  - OPEN Alliance TC14 Interoperability Specifications
  - OPEN Alliance TC14 EMC Specifications
  - OPEN Alliance TC14 System Implementation
- Compatibility with any Clause 4 compliant MAC
- Optimized for very low latency and low TO_TIMER
- Enhanced Noise Immunity PMA operation (ENI)
- TX/RX SFD detection
- False Carrier signaling over MII
- Collision detection masking
- PCS and PMA loopback mode
- PCS remote jabber detection
- PCS reflection mode
- PLCA Precedence Mode
- PLCA RX FIFO Mode
- PLCA leader (coordinator) selection
- Configurable PLCA Burst Mode
- Optional MDIO Clause 22 slave module
- Optional PLCA BEACON/COMMIT extensions over MII
- Optional PCS “Unjab” timer support

Description

The CT25205 Digital IP core provides the PMA, PCS, and PLCA Reconciliation Sublayer building blocks of a standard IEEE 802.3cg® 10BASE-T1S Ethernet Physical Layer.

The RTL code is written in plain Verilog 2005 HDL, and it is fully synthesizable on standard cells and FPGA systems. It works in conjunction with any standard IEEE CSMA/CD Clause 4 Ethernet MAC using MII.

The integrated PLCA RS allows existing MAC devices that do not support the new PLCA MII extensions to take advantage of the PLCA advanced features. On the other end, the PMA connects to a standard OPEN Alliance 10BASE-T1S PMD Interface.

The CT25205 can be used in conjunction to other analog and digital blocks like (a) the CT25203 to implement a complete physical layer ethernet device, (b) the CT25208 to implement a digital MACPHY and (c) the CT25203, the CT25208 and the CT25209 to implement a complete OPEN Alliance MACPHY (see next page for details).

CT25207

OPEN Alliance TC14 10BASE-T1S PMD Controller

Status

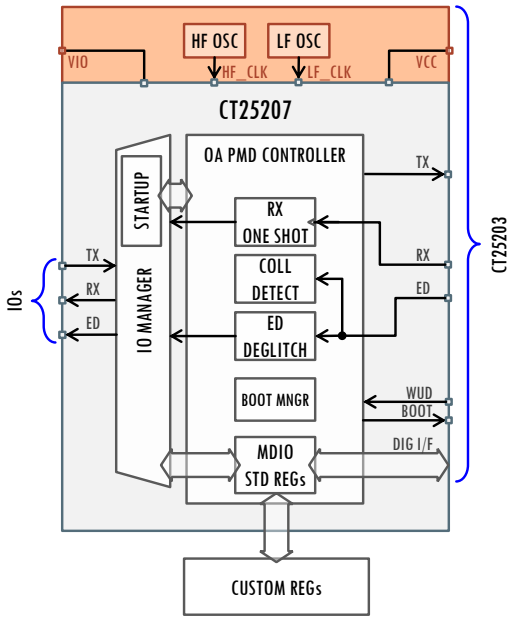
- Under development (silicon-proven by Q2-2023)

Deliverables

- RTL Object-Code
- Integration-level Verification Env. (UVM)
- Coverage Report
- SDC Constraints
- Integration Guide
- Test Specifications

Applications

- Automotive Networks
- Industrial Networks



Features

- Compliant to:
  - OPEN Alliance TC14 10BASE-T1S PMD I/F
  - OPEN Alliance TC14 Interoperability Specifications
  - OPEN Alliance TC14 System Implementation
  - OPEN Alliance TC10 Wake Up detection
  - OPEN Alliance TC14 Topology discovery
- Low Power consumption meeting OPEN Alliance TC10 requirement in sleep mode
- VCC supply 3.3V supply (±10%)
- VIO supply 2.5V or 3.3V (±10%)
- Voltage and current references, test infrastructures, included
- 10MHz (±30%) and 210MHz (±8%) input clocks for operation (oscillators available upon request in the target silicon process)

Description

The CT25207, in combination with the CT25203, implements a complete OPEN Alliance TC14 10BASE-T1S PMD Interface. The IP's tasks are:

- perform the boot sequence and drive the platform outside the IP to do the proper startup sequence after POR and after WAKE request
- recognize the encoded TX commands and keep updated the state of the PMD FSM after boot
- drive the platform outside the IP to do the shutdown sequence to enter LOWPOWER mode
- Filter ED and RX to fulfill the requirements of OPEN Alliance TC14 10BASE-T1S PMD I/F
- detect collisions on the line when transmitting and signal them on ED pin
- generate TX pulses for Topology Discovery with proper PRBS sequence
- perform WUT validation for wake-up

The IP also includes a MDIO slave that allows access to Clause 22 PMD standard registers and to IP specific registers (both embedded in the IP) and to custom registers (to be placed outside the IP).

CT25208

IEEE 802.1® Clause 4 "Tiny" MAC

Status

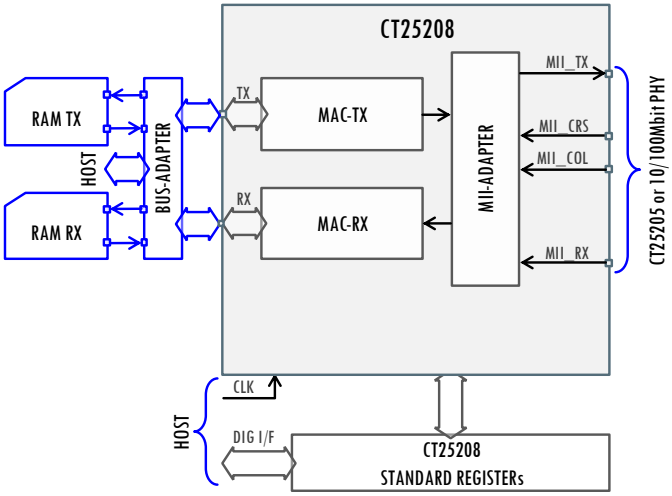
- Silicon-Proven
- Fully characterized
- In mass production

Deliverables

- RTL Object-Code
- Integration-level Verification Env. (UVM)
- Protocol Compliance & Coverage Report
- SDC Constraints
- Integration Guide

Applications

- Automotive Networks
- Industrial Networks



Features

- Full CSMA/CD compliance, including half and full-duplex
- Support for 10 and 100 Mb/s operation
- Single MAC address filtering
- Promiscuous Mode
- FCS add/check
- Diagnostic Counters
- Status reporting
- Multiple MAC address filtering (multicast) based on address/mask pairs
- Broadcast / Multicast filtering
- Configurable FCS checking
- Underrun/Overrun error handling
- Disable of back-off mechanism

Description

The CT25208 Digital IP core is a standard Clause 4 CSMA/CD MAC exposing a proprietary, FIFO-like MAC Client interface (TX/RX).

On the other end, the CT25208 features a proprietary, MII-like Reconciliation Sublayer (RS) interface, including adapter modules to interface with standard MII/RMII PHYs.

The RTL code is written in plain Verilog 2005 HDL, and it is fully synthesizable on standard cells and FPGA systems.

The flexible MAC Client interface can also be configured for transferring 1, 2, or 4 bytes at a time, supporting both little-endian and big-endian byte order. This feature allows the CT25208 IP to be used with many MCUs and other systems based on shared-memory access by means of a dedicated Bus Adapted interface.

The CT25208 can be used in conjunction to others analog and digital blocks like (a) the CT25205 to implement a digital 10BASE-T1S MACPHY and (b) the CT25203, the CT25205 and the CT25209 to implement a complete OPEN Alliance MACPHY (see next page for details).

CT25209

OPEN Alliance TC6 10BASE-T1S MACPHY Interface

Status

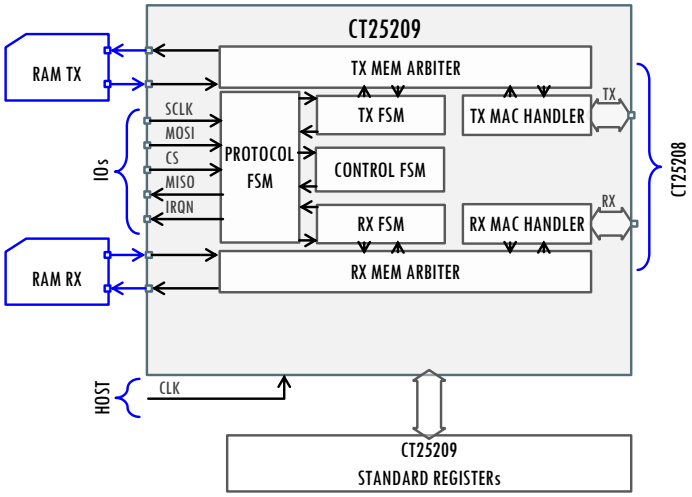
- Silicon-Proven
- Fully characterized
- In mass production

Deliverables

- RTL Object-Code
- Integration-level Verification Env. (UVM)
- Protocol Compliance & Coverage Report
- SDC Constraints
- Integration Guide

Applications

- Automotive Networks
- Industrial Networks



Features

- Compliant to the OPEN Alliance TC6 Serial 10BASE-T1x MACPHY Interface specifications
- Support for 8, 16, 32 and 64 bytes chunks
- Support for both Store & Forward and Cut-Through operating mode
- Protected and Unprotected control transactions
- Transmit FCS verification

Description

CT25209 Digital IP core implements the MACPHY SPI protocol defined by the “OPEN Alliance TC6 Serial 10BASE-T1x MACPHY Interface specifications”.

The top-level block exposes an industry-standard, slave Serial Peripheral Interface (SPI) towards an host controller such as a microprocessor or an Ethernet switch. On the other end, the CT25209 features a proprietary FIFO-like MAC Client interface (TX/RX) which can be easily adapted to many existing Ethernet MAC IPs or connected directly to the CT25208 10/100 Mbps Ethernet MAC IP.

The RTL code is written in plain Verilog 2005 HDL, and it is fully synthesizable on standard cells and FPGA systems.

The CT25209 can be used in conjunction to the CT25203, the CT25205 and the CT25208 to implement a complete OPEN Alliance TC6 MACPHY.

CT25205_TC

10BASE-T1S PHY/PMD Test Chip Vehicle

Description

The CT25205_TC is an IEEE 10BASE-T1S Physical Layer Transceiver supporting operation over a multi-drop network with at least 8 nodes and up to 25m of overall single twisted-pair cable length.
It supports MII to interface with a standard CSMA/CD compliant Ethernet MAC running at 10 Mb/s and the OPEN Alliance three-pin PMD Interface. It integrates the PLCA (**Physical Layer Collision Avoidance**) reconciliation sublayer functions to avoid physical collisions on the bus.
PLCA improves CSMA/CD performance in several ways:

- Guarantees that a packet transmitted by the MAC meets the line within a known time (bounded latency)
- Assigns transmit opportunities in a round-robin fashion to ensure fair access to the medium
- Maximizes throughput by avoiding collisions and MAC multiple back-off / retry
- Provides protection against the “babbling idiot” problem
- Allows for more robust operations in automotive EMC environment
- Integrating the PLCA RS in a single PHY chip allows existing SoC and MAC ICs to take advantage of PLCA

CT25205_TC Features

- Compliant to IEEE 802.3cg
- Integrated PLCA Reconciliation Sub-Layer
- Supports Short Reach Half-Duplex, Point-to-Point mode and Half-Duplex, Multi-Drop mode
- MII Interface support
- OA PMD Interface support
- MIIM (MDC/MDIO) Mngt Bus up to 2.5MHz
- Clause 45 Address Space
- Supports Clause 22 to Clause 45 access mode
- Interrupt Pin Option
- Robust Operation Over Single Twisted-Pair Automotive Cables
- Sustains OA DPI test @39dBm, maintaining a BER less than 10^{-10}
- Meets OA Automotive Emission Limits
- Single 5V power supply
- Adjustable 2.5V-5V I/O Supply
- Low Power < 200mW
- -40°C to 125°C Temp. range
- Experimental test chip not to be used in series production

36-pin QFN Package (6x6mm)

CT25205_TC Pinout

1	AIO0 Reserved test Pin	10	DIO1 General Purposes IO	19	TXD[0] MII Interface	28	RXER MII Interface
2	XTALO XTAL term	11	DIO0 General Purposes IO	20	TXD[1] MII Interface	29	RXDV MII Interface
3	XTALI XTAL term / ck input	12	MDINT MIIM interrupt signal	21	TXD[2] MII Interface	30	RXD[0] MII Interface
4	AVDDIN 5V Supply	13	RST Active Low Reset	22	TXD[3] MII Interface	31	RXD[1] MII Interface
5	PVDDIN 5V Supply	14	MDCK MDIO clock input	23	VDDIO 2.5V to 5.0V IO Supply	32	RXD[2] MII Interface
6	DRVVDD_P Internal LDO Output	15	MDIO MDIO open-drain IO	24	DVDD Internal LDO Output	33	RXD[3] MII Interface
7	LINEP Positive Line Pin	16	TXCK MII Clock	25	RXCK MII Interface	34	FSOURCE Reserved test Pin
8	LINEN Negative Line Pin	17	TXEN MII Interface	26	CRS MII Interface	35	AVDDIN 5V Supply
9	DRVDD_N Internal LDO Output	18	TXER MII Interface	27	COL MII Interface	36	AIO1 Reserved test Pin

10BASE-T1S

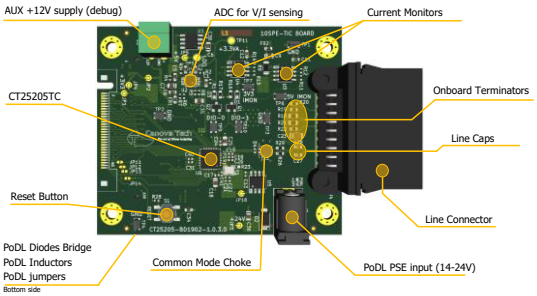
Evaluation and Development boards

Description

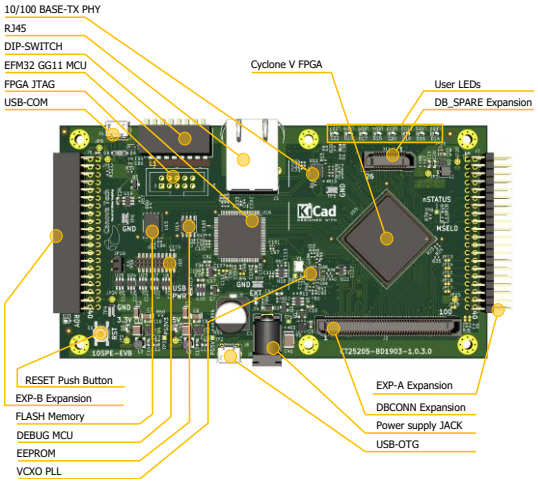
CT25205-BD1903 motherboard together with the CT25205-BD1902 expansion card form the Canova Tech CT25205TC 10BASE-T1S multidrop Ethernet PHY evaluation board.

The evaluation system features a command line interface allowing the user to manage the chip configuration and to perform different kind of basic tests. The board can also serve as a starting point for application development.

BD1902 Daughterboard



BD1903 Motherboard



Features

- CT25205_TC – World first 10BASE-T1S PHY IC including PLCA Reconciliation Sublayer
- MQP Automotive Line Connector
- Supports engineered PoDL
- -40/+125 °C operating temperature range
- CMC for extended EMI performance
- Onboard current/voltage monitors including ADC

- Silicon Labs EFM32 Giant Gecko MCU
  - TQFP-100 package, 2048 kB Flash, 512 kB RAM
- Intel Cyclone V FPGA
  - 25 k Cells, 9434 LABs/CLBs, 2002944 RAM bits
- 0/+85 °C operating temperature range
- 100 pins DB expansion connector
- 2x40 pin expansion header
- Debugger/Programmer connectors for microcontroller and FPGA
- Power sources include USB and external supply from DB
- USB Micro-B connector usable as standard COM port
- USB Micro-B connector (host and device mode)
- 10/100 BASE-TX Ethernet PHY with standard RJ-45 connector
- 32 MB Flash Memory with SPI interface
- 2kbit EEPROM with I2C interface and 48bit Unique Node Address
- 25MHz Crystal connected to I2C progr. clock generator with VCXO
- 8 configuration dip-switches
- 8 user-defined LEDs

Status

- CT25205TC test chip samples available to be shipped
- BD1902 Daughterboards are available to be shipped
- The BD1902 can be modified to fit the mechanical and connector routing of the customer's application

- BD1903 Motherboards are available to be shipped